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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,667	04/21/2004	Roxanne Vu	EV 391867051 US	4915

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DENIRO/RAMBUS
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EXAMINER	
COX, CASSANDRA F	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary	Application No.	Applicant(s)	
	10/828,667	VU ET AL.	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4/21/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-30* is/are allowed.

6)☒ Claim(s) *1-2, 11-13, 31-32, 35, 38* is/are rejected.

7)☒ Claim(s) *3-10,33,34,36 and 37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/19/04,7/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the adjustable resistor included in the filter (with respect to claim 5) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 11, 31-32, and 35 are rejected under 35 U.S.C. 102(b) as being anticipated by Taketoshi et al. (U.S. Patent No. 5,389,898).

In reference to claim 1 Taketoshi discloses in Figure 1 a phase locked loop circuit comprising: a phase-frequency detector (shown as the detector of circuit 1) capable of providing a phase difference signal responsive to an input signal and a feedback signal; a charge pump (shown as part of circuit 1, the inverter, pmos and nmos transistor) coupled to the phase frequency detector, capable of providing a first voltage (Vpc) responsive to the phase difference signal; a filter (2), coupled to the charge-pump, capable of providing a second voltage (Vcnt) responsive to the first voltage (Vpc); a first voltage-controlled oscillator (VCO1), coupled to the filter (2), capable of providing the feedback signal responsive to the second voltage (Vcnt); and a second voltage-controlled oscillator (VCO2), coupled to the filter (2), capable of providing the feedback signal responsive to the second voltage (Vcnt). The same applies to claims 31-32.

In reference to claim 2, Taketoshi discloses in Figure 1 the circuit further comprising a multiplexer (4), coupled to the first (VCO1) and second (VCO2) voltage-controlled oscillators, capable of providing the feedback signal responsive to a control

signal (SELECTION CONTROL). The same applies to claim 35 and 38 (wherein the means is considered to be the multiplexer).

In reference to claim 11, the filter (2) is considered to be a low-pass filter.

4. Claims 1, 11, and 31-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakanishi et al. (U.S. Patent No. 6,188,285).

In reference to claim 1 Nakanishi discloses in Figure 1 a phase locked loop circuit comprising: a phase-frequency detector (shown as the detector of circuit 1) capable of providing a phase difference signal responsive to an input signal and a feedback signal; a charge pump (shown as part of circuit 1) coupled to the phase frequency detector, capable of providing a first voltage responsive to the phase difference signal; a filter (2), coupled to the charge-pump, capable of providing a second voltage (VL) responsive to the first voltage; a first voltage-controlled oscillator (5), coupled to the filter (2), capable of providing the feedback signal responsive to the second voltage (VL); and a second voltage-controlled oscillator (15), coupled to the filter (2), capable of providing the feedback signal responsive to the second voltage (VL). The same applies to claims 31-32.

In reference to claim 11, the filter (2) is a low-pass filter.

5. Claims 1-2 and 31-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Welland (U.S. Patent No. 6,304,146).

In reference to claim 1 Welland discloses in Figures 2 and 14 a phase locked loop circuit comprising: a phase-frequency detector (206) capable of providing a phase difference signal responsive to an input signal and a feedback signal; a charge pump

(208) coupled to the phase frequency detector, capable of providing a first voltage responsive to the phase difference signal; a filter (210), coupled to the charge-pump, capable of providing a second voltage (Vc) responsive to the first voltage; a first voltage-controlled oscillator (VCO1), coupled to the filter (210), capable of providing the feedback signal responsive to the second voltage (Vc); and a second voltage-controlled oscillator (VCO2), coupled to the filter (210), capable of providing the feedback signal responsive to the second voltage (Vc). The same applies to claims 31-32.

In reference to claim 2, Welland discloses in Figure 14 the circuit further comprising a multiplexer (1410), coupled to the first (VCO1) and second (VCO2) voltage-controlled oscillators, capable of providing the feedback signal responsive to a control signal (the signal for controlling the opening and closing of the switch, which is not shown but considered to be inherent). The same applies to claims 35 and 38 (wherein the means is considered to be the multiplexer).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taketoshi et al. (U.S. Patent No. 5,389,898) in view of Arawal et al. (U.S. Patent No. (6,650,141).

In reference to claim 12 Taketoshi discloses all the limitations of the claim with respect to claim 1 (as mentioned above), except Taketoshi does not disclose that the phase locked loop circuit is coupled to a serializer circuit and a deserializer circuit. Agrawal discloses in Figure 9 a phase locked loop circuit (190) coupled to a serializer circuit (186) and a deserializer circuit (184). It would have been obvious to one skilled in the art at the time of the invention that the phase locked loop of Taketoshi could be used in the circuit of Agrawal (since Agrawal does not disclose a particular PLL design) for the advantage of providing an improved PLL capable of realizing high-speed pulling even if the frequency variable-range of that PLL is expanded (see column 1, lines 65-68).

In reference to claim 13, the circuit of Agrawal is seen to be included in a memory device.

8. Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakanishi et al. (U.S. Patent No. 6,188,285) in view of Arawal et al. (U.S. Patent No. (6,650,141).

In reference to claim 12 Nakanishi discloses all the limitations of the claim with respect to claim 1 (as mentioned above), except Nakanishi does not disclose that the phase locked loop circuit is coupled to a serializer circuit and a deserializer circuit. Agrawal discloses in Figure 9 a phase locked loop circuit (190) coupled to a serializer circuit (186) and a deserializer circuit (184). It would have been obvious to one skilled in the art at the time of the invention that the phase locked loop of Nakanishi could be used in the circuit of Agrawal (since Agrawal does not disclose a particular PLL design)

for the advantage of providing a phase-locked loop circuit and a voltage-controlled oscillator having a plurality of frequency ranges of oscillations that can be produced and a small power consumption (see column 2, lines 49-52).

In reference to claim 13, the circuit of Agrawal is seen to be included in a memory device.

9. Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Welland (U.S. Patent No. 6,304,146) in view of Arawal et al. (U.S. Patent No. (6,650,141).

In reference to claim 12 Welland discloses all the limitations of the claim with respect to claim 1 (as mentioned above), except Welland does not disclose that the phase locked loop circuit is coupled to a serializer circuit and a deserializer circuit. Agrawal discloses in Figure 9 a phase locked loop circuit (190) coupled to a serializer circuit (186) and a deserializer circuit (184). It would have been obvious to one skilled in the art at the time of the invention that the phase locked loop of Welland could be used in the circuit of Agrawal (since Agrawal does not disclose a particular PLL design) for the advantage of providing an PLL capable of synthesizing high-frequency signals while overcoming integration problems associated with prior art phase locked loops (see column 3, lines 30-35).

In reference to claim 13, the circuit of Agrawal is seen to be included in a memory device.

Allowable Subject Matter

10. Claims 14-30 are allowed.

11. Claims 3-10, 33-34, and 36-37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter: Claims 3-4, 6, 33, and 37 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 5 wherein the charge pump (500) includes an adjustable gain responsive to a control signal (FreqSel) in combination with the rest of the limitations of the base claims and any intervening claims. Claims 5 and 34 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 2 wherein the filter (203) includes an adjustable resistor responsive to a control signal (FreqSel) in combination with the rest of the limitations of the base claims and any intervening claims. Claims 7-8 and 36 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 2 wherein the circuit further comprises a voltage regulator (204) coupled to the filter (203) and the first (205) and second (206) voltage-controlled oscillators in combination with the rest of the limitations of the base claims and any intervening claims. Claim 9 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 2 wherein the circuit further comprises a phase mixer (207) coupled to the first (205) and second (206) voltage-controlled oscillators in combination with the rest of the limitations of the base claims and any intervening claims. Claim 10 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 2 wherein the circuit further comprises a clock buffer (207) coupled to the first (205) and second (206)

voltage-controlled oscillators in combination with the rest of the limitations of the base claims and any intervening claims.

13. The following is an examiner's statement of reasons for allowance: Claims 14-22 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 3 wherein the circuit also comprises an amplifier (204), coupled to the filter (203) and a multiplexer (301) coupled to the amplifier (204) in combination with the rest of the limitations of the base claims and any intervening claims. Claims 23-30 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 4 wherein the circuit includes a first amplifier (401) and a second amplifier (402) in combination with the rest of the limitations of the base claims and any intervening claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CC

May 29, 2005

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